HITACHI

APPLICATION NOTE

HITACHI POWER MOS FET

HITACHI SEMICONDUCTOR

1. Features of Power MOS FETs

In developing power MOS FETs, Hitachi took note of the outstanding characteristics of small signal MOS FETs used for high frequency amplification in TV tuners and FM tuners. After intensive research, we perfected high-output MOS FETs and introduced them as commercial products.

Hitachi's power MOS FETs have the line-up shown in Table 1-1. Each pair consists of an N channel type and a P-channel type, which have complementary characteristics.

MOS FETs have the following advantages:

- Require a very low driving power as they are voltage-controlled devices.
- Free from current concentration, and hence have enormous resistance to destruction.
- Good frequency response and high switching speed due to absence of carrier storage effect.

These advantages make for the outstanding characteristics of power amplification devices. On the other hand, it is difficult to provide MOS FETs with the high voltage and high current characteristics required of power amplifiers. Hitachi succeeded in imparting these characteristics to MOS FETs by the method described in a later section of this application note.

Table 1-1 Series and Maximum Ratings of Power MOS FET

Type		Outline	I_D (A)	V_{DSX} (V) (V_{DSS} (V))	Peh * (W)
N-Channel	P-Channel				
2SK133	2SJ48	JEDEC: TO-3 EIAJ: TC-3, TB-3	7	120	100
2SK134/Ⓗ	2SJ49/Ⓗ		7	140	100
2SK135/Ⓗ	2SJ50/Ⓗ		7	160	100
2SK175/Ⓗ	2SJ55/Ⓗ		8	180	125
2SK176/Ⓗ	2SJ56/Ⓗ		8	200	125
2SK220Ⓗ	–		8	(160)	100
2SK221Ⓗ	–		8	(200)	100
2SK225	2SJ81	HPAK	7	120	100
2SK226	2SJ82		7	140	100
2SK227	2SJ83		7	160	100
2SK213	2SJ76	JEDEC: TO-220AB EIAJ: SC-46	0.5	140	30
2SK214	2SJ77		0.5	160	30
2SK215	2SJ78		0.5	180	30
2SK216	2SJ79		0.5	200	30

* Value at Tc=25°C

8.1 Audio Power Amplifiers

(1) Basic design philosophy

• Frequency characteristics (frequency vs. gain, phase)

The output stage of an ordinary power amplifier uses a push-pull emitter follower (source follower). This method is popular because it provides a wider transfer bandwidth and more stable operation than other grounding systems.

Meanwhile, the forward transconductance (forward transfer admittance) y_{fs} of power MOS FETs is as large as 1.0 S (siemens). Yet it is only a fraction of that of general bipolar transistors and this represents a disadvantage in terms of open loop distortion. The reason is that when bipolar transistors are used as an emitter follower, y_{fs} is given as:

$$y_{fs} = 1/r_e = \frac{I_E}{KT/q}$$

where r_e = Emitter equivalent resistance
K = Boltzmann constant
T = Absolute temperature
q = Electron charge
I_E = Emitter bias current
R_L = Load resistance

Even when I_E is 1 A, for instance, $y_{fs} \doteqdot 40$ S.

Now the relationship between input and output is

$$e_o/e_i = \frac{R_L}{R_L + 1/y_{fs}}$$

and the nonlinier component of y_{fs} causes distortion, so that a larger y_{fs} is of greater advantage. In other words, since a power MOS FET has a distortion about 20 dB larger than a bipolar transistor, it is necessary to use a larger open loop gain and a larger negative feedback than a bipolar transistor. As shown by the frequency characteristics in Fig. 3-4, however, a Darlingoton connection must be used for bipolar transistors in order to enlarge the bandwidth, so that the two-stage emitter follower would worsen the phase characteristics. In applying a negative feedback, a large phase shift would force a sacrifice of gain frequency characteristics in a phase compensation circuit and the like. Thus, with a source follower with a single power MOS FET, much feedback can be applied over a large bandwidth, and distortion can be reduced.

The driver stage of a power MOS FET does not require a conventional class B driver stage. Therefore, the poles in the amplifier system can be reduced and a stable negative feedback amplifier can be formed.

In the frequency characteristics of open loop gain, setting the peak value near 10 ~ 20 kHz is the key to forming a good circuit.

Setting the peak value at the upper limit of the audible range is impossible with conventional bipolar transistors. This can be realized only by using power MOS FETs with excellent high-frequency and switching characteristics.

Fig. 8-1 shows the difference in open loop gain of audio amplifiers designed with power MOS FETs and bipolar transistors.

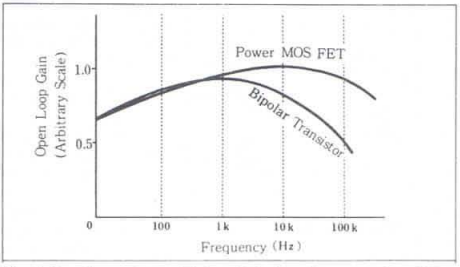

Fig.8-1 Open Loop Gain of Audio Power Amplifier

• Consideration for parastic oscillation

As power MOS FETs have excellent high-frequency characteristics, they are liable to cause oscillation when used in high-gain designs such as described in the preceding section. To avoid this, a gate resistance (200 ~ 500 Ω) may be used to prevent a real part of the input impedance to be negative. Or the gate wiring pattern may be minimized (within 5 cm), as stated in the section on precautions in fabrication later in this manual. Or one-point grounding may be used.

When a gate resistance is inserted, frequency characteristics are worsened as shown in Fig. 8-2, so that optimum values must be selected in designing. The gate resistance will have no effect in case the former stage has a high impedance as in a class A driver stage.

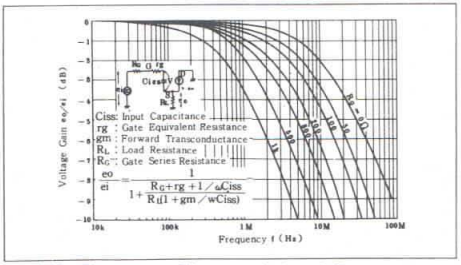

Fig.8-2 Frequeney Characteristies of Source Follower (Calculated Value)

(2) Typical design – 1 (100 W output at 100 kHz, 0.01%)

A circuit is shown in Fig. 8-3. Design of each amplifier stage will be discussed below.

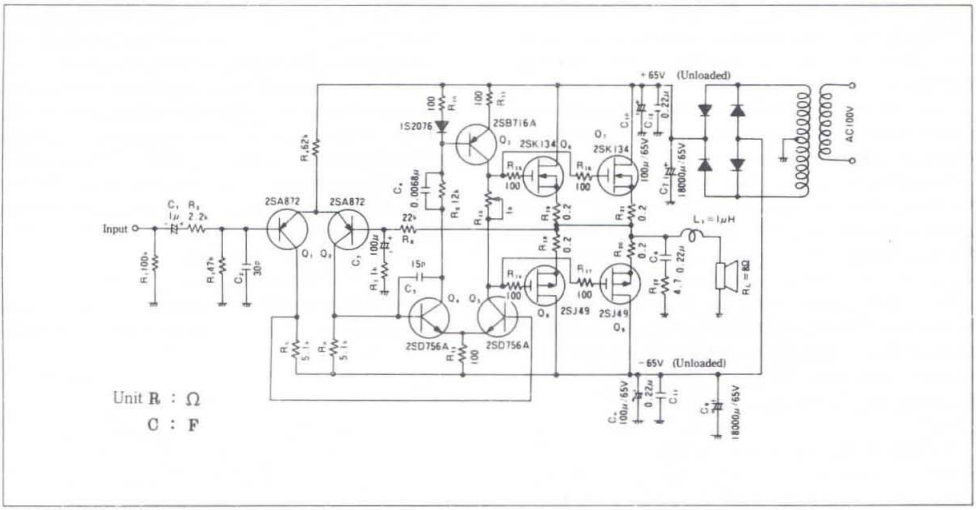

Fig.8-3 Full Circuit of 100 W Output Audio Amplifier

• Design of output stage

Fig. 8-4 shows an equivalent circuit of the output stage for N channel MOS FETs. R_{ON} is a drain-to-source equivalent resistance when the power MOS FET is on. The resistance 1.71Ω contains some margin as it was calculated for the worst case from the specifications for 2SK135 and 2SJ50.

$$R_{ON} = \frac{V_{DS(sat)}}{I_D} = \frac{12}{7} \fallingdotseq 1.71\ (\Omega)$$

Peak current I_p flowing in load R_L = 8 Ω at P_O = 100 W is calculated from mean current I,

$$P_O = I^2 \cdot R_L\ ,\ I_p = \sqrt{2} \cdot I,$$

$$\text{as } I_p = \sqrt{2} \cdot \sqrt{\frac{P_O}{R_L}} = \sqrt{2} \cdot \sqrt{\frac{100}{8}} \fallingdotseq 5\ \text{A}.$$

Therefore, if transformer regulation is estimated as 20% and AC line regulation as ±15%, then power supply voltage V_{DD} is given as

$$V_{DD} = 1.2 \times 1.15\ \{R_L + 0.5\ (R_{ON} + R_S)\} \times I_p \fallingdotseq 61.8\text{V}.$$

In Fig. 8-3, the voltage is set at ±65 V including a margin.

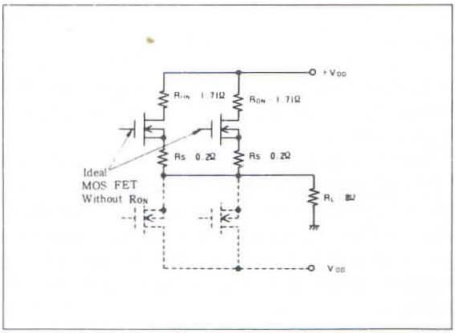

Fig.8-4 Equivalent Circuit of the Output Stage for N-Channel Power MOS FETs

• Design of voltage amplifier stage

A power MOS FET can be used with a low driving power. Fundamentally, only the power for charging and discharging the gate-to-source capacitance is needed to the output stage, so that no class B driver stage is required.

The driving power varies with input frequency. At 100 W output and 10 kHz frequency, it would be about 10 mW.

Therefore, an output stage power MOS FET can be driven directly from a class A predriver (voltage amplifier stage) used in a bipolar transistor amplifier. By eliminating the class B driver, the number of components can be reduced, and impairing the amplifier's performance caused by the driver itself can be avoided. Further, the number of poles for transfer function (open loop gain vs. frequency characteristics) decrease, and the stagger can easily be increased. Consequently, the stability against oscillation is improved.

Transistors for the voltage amplifier stage are required to have a high voltage durability, low C_{ob}, and high f_T. Here the 2SD756A/2SB716A developed especially for power MOS FETs are used. With the NPN differential amplifier and PNP constant current load, high gain and low distortion characteristics were obtained.

The class A stage bias current is set as 10 mA. When bias current is lacking, sufficient power to drive a power MOS FET at high frequency cannot be supplied, and distortion would worsen.

The drain current temperature coefficient of a power MOS FET undergoes a reversal of polarity at around I_D = 100 mA and temperature compensation in the large current region will be unnecessary. Hence, the bias circuit for a power MOS FET is vastly simplified because only one semifixed resistor (1 kΩ) for setting idling current will suffice.

• Design of input stage circuit

For the input stage, a stable differential amplifier circuit was formed by using the high-voltage, low-noise transistor 2SA872, which is known for its high performance in improving the S/N ratio. Bias current is set as 0.5 mA.

• Typical characteristics of experimental circuit (Fig. 8-3)

Output vs. distortion characteristics are shown in Fig. 8-5. At f = 1 kHz, total harmonic distortion (THD) is approximately 0.002%, which is the limit value for any measuring system available on the market today.

Through optimum design, the following can be obtained at rated output:

f = DC ~ 100 kHz,
THD ≦ 0.01%

Thus, characteristics that cannot be obtained with conventional bipolar transistors are realized with power MOS FETs.

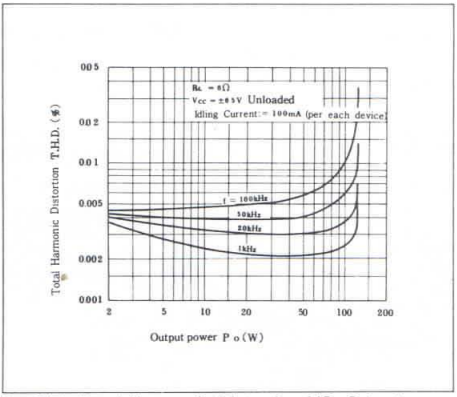

Fig.8-5 Total Harmonic Distortion VS. Output Characteristics

• Precautions in fabrication

- Minimize the gate wiring, although its relationship with gate resistance must be taken into consideration.
- Provide one-point grounding for the amplifier base plate, power supply, chemical fapacitor to prevent ± line unbalance, and speaker terminals.
- The output coupling coil has the effect of reducing distortion in the high frequency range, and preventing abnormal oscillation in capacitance loaded operation. But the values should be determined while experimenting.

(3) Typical design – 2 (50 W output at 50 kHz, 0.01%)

Introduced here is a power amplifier with a rated output of 50 W and which attains a total harmonic distortion of 0.01% over the entire frequency bandwidth of from 5 Hz to 50 kHz. The basic design method has been introduced in the previous section. The output stage, as shown in Fig. 8-6, is of the single push-pull construction. Considering the power supply voltage and transformer regulation, the complementary pair 2SK133/2SJ48 would suffice as the power MOS FETs to be used.

This circuit can produce an output of about 70 W by improving transformer regulation or stabilizing the power supply line.

In the frequency characteristics of open loop gain, the peak point is set at 10 kHz, 100 dB. Even at 100 kHz, a high gain of 85 dB is ensured.

Fig. 8-7 shows the distortion vs. output characteristics with the experimental circuit.

In this high negative feedback amplifier, caution must be taken to avoid the oscillation which depends on the printed pattern.

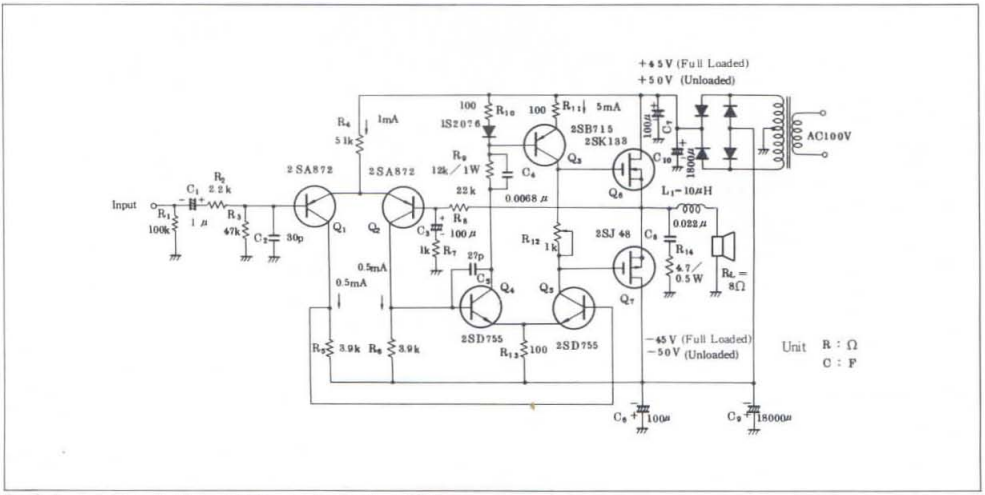

Fig.8-6 Full Circuit of 50W Output Audio Amplifier

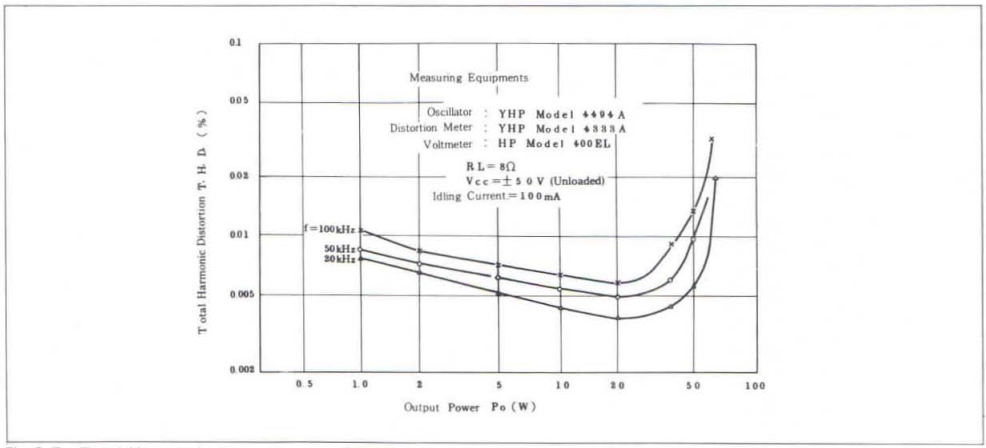

Fig.8-7 Total Hormonic Distortion vs. Output Characteristics

Fig. 8-8 shows the standard printed pattern. The amplifier devices that drive the output stage power MOS FETs consist only of five small-signal transistors, so that the printed board is extremely small.

Wiring between the voltage amplifier stage collector and the power MOS FET gate must be minimized. The arrangement and configuration of the printed board and the heat sink must be selected carefully.

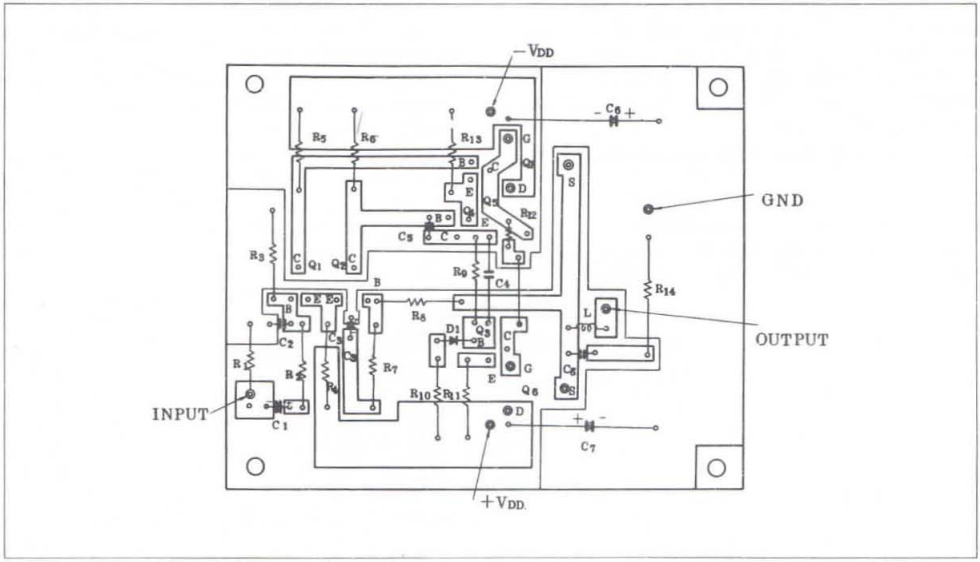

Fig.8-8 Standard Printed Pattern in Actual Size

In Fig. 8-8 which shows the example of the printed board pattern, the printed board is attached directly to the heat sink to minimize the gate wiring.

(4) Recommended line-up by output power

Line-up of devices in audio amplifiers of different outputs is shown Table 8-1.

Table 8-1 Line-up of Devices in Audio Power Amplifier

Output Power (W)	Input Stage		Driver Stage		Output Stage					V_{DSX} (V)
	N-Channel (NPN)	P-Channel (PNP)	N-Channel (NPN)	P-Channel (PNP)	Connection	TO-3		HPAK		
						N-Channel	P-Channel	N-Channel	P-Channel	
50~80	2SK151 (TO-92MOD.)	2SJ51 (TO-92MOD.)	2SK213 (TO-220AB)	2SJ76 (TO-220AB)	Single Push-Pull	2SK133	2SJ48	2SK225	2SJ81	120
	2SC1775 (TO-92)	2SA872 (TO-92)	2SD756 (TO-92MOD.)	2SB716 (TO-92MOD.)						
			2SD756A (TO-92MOD.)	2SB716A (TO-92MOD.)		2SK134	2SJ49	2SK226	2SJ82	140
			2SK214 (TO-220AB)	2SJ77 (TO-220AB)						
100~140	2SC1775 (TO-92)	2SA872 (TO-92)	2SD758 (TO-202AA MOD.)	2SB718 (TO-202AA MOD.)		2SK175	2SJ55	–	–	180
			2SK216 (TO-220AB)	2SJ79 (TO-220AB)						
			2SD666A (TO-92MOD.)	2SB646A (TO-92MOD.)	Parallel Push-Pull	2SK134	2SJ49	2SK226	2SJ82	140
			2SK214 (TO-220AB)	2SJ77 (TO-220AB)						
			2SD668A (TO-126MOD.)	2SB648A (TO-126MOD.)		2SK135	2SJ50	2SK227	2SJ83	160
			2SK215 (TO-220AB)	2SJ78 (TO-220AB)						
150~200	2SC1775A (TO-92)	2SA872A (TO-92)	2SD758 (TO-202AA MOD.)	2SB718 (TO-202AA MOD.)		2SK176	2SJ56	–	–	200

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